WHAT IS CLAIMED IS:

1. A method of writing data in an EEPROM using a single supply voltage, the EEPROM including a memory cell array having a plurality of memory cells, each memory cell comprising a storage transistor having a source and a drain, a floating gate and a control gate disposed over the floating gate, said method comprising steps of:

applying a first voltage higher than both the supply voltage and a ground voltage to at least one of the source and drain of the storage transistor of each of selected memory cells; the first voltage being generated from the single supply voltage;

applying a second voltage lower than both the supply voltage and the ground voltage to the control gate of the storage transistor of each of the selected memory cells while the first voltage is applied to at least one of the source and drain, whereby electrons are released from the floating gate when both the first and second voltages are applied, the second voltage being generated from the single supply voltage.

2. The method of claim 1, wherein a potential difference between said first and second voltages is sufficient to cause electrons to tunnel out of said floating gate.

3. The method of claim 1, wherein each of said memory cells also comprises a select transistor connected in series with said storage transistor, said select transistor also has a source and a drain, and said select transistor has a source-drain breakdown voltage equal to or greater

than said first voltage, and a potential difference between said first voltage and said second voltage is greater than said source-drain breakdown voltage.

4. The method of claim 1, wherein each of said memory cells additionally comprises a select transistor connected in series with said storage transistor, said select transistor has a source and a drain and a source/drain-junction breakdown voltage equal to or greater than said first voltage, and a potential difference between said first voltage and said second voltage is larger than said source/drain-junction breakdown voltage.

5. The method of claim 1, wherein said method further comprises the steps of:

generating said first voltage from said supply voltage and said ground voltage; and

generating said second voltage from said supply voltage and said ground voltage.

6. The method of claim 1, wherein each of said memory cells additionally comprises a select transistor connected in series with said storage transistor, said select transistor has a source and a drain, and a source-drain breakdown voltage and a source/drain-junction breakdown voltage, and the source-drain breakdown voltage of the select transistor and the source/drain-junction breakdown voltage of the select transistor are each less than the potential difference between the first and second voltages.

7. The method of claim 1, and further including reading data from each of said memory cells by applying the supply voltage to the control gate and applying the ground to one of the source and drain during the reading of the data from the memory cell.

8. The method of claim 1, further comprising;

applying said ground voltage to at least one of the source and drain of the storage transistor of a non-selected memory cell,

whereby data is written in said selected memory cells simultaneously.

9. The method of claim 1, wherein said storage transistor also includes a substrate having a first conductivity type provided therein with said source and drain, said source and drain being of a second conductivity type.

10. The method of claim 9, wherein said substrate is biased to a voltage equal to or higher than said second voltage.

11. A method of writing data in an EEPROM using a single supply voltage, the EEPROM including a memory cell array having a plurality of memory cells, each memory cell comprising a storage transistor having a source and a drain, a floating gate and a control gate disposed over the floating gate, said method comprising steps of:

applying a first voltage higher than both the supply voltage and a ground voltage to at least one of the source and drain of the storage transistor of each of selected memory cells; the first voltage being generated from the single supply voltage by using a first built-in charge pump circuit;

applying a second voltage lower than both the supply voltage and the ground voltage to

the control gate of the storage transistor of each of the selected memory cells while the first voltage is applied to at least one of the source and drain, whereby electrons are released from the floating gate when both the first and second voltages are applied, the second voltage being generated from the single supply voltage by using a second built-in charge pump circuit.

12. The method of claim 11, wherein said substrate is biased to a voltage equal to or higher than said second voltage.

13. The method of claim 11, wherein a potential difference between said first and second voltages is sufficient to cause electrons to tunnel out of said floating gate.

14. The method of claim 11, wherein each of said memory cells also comprises a select transistor connected in series with said storage transistor, said select transistor also has a source and a drain, and said select transistor has a source-drain breakdown voltage equal to or greater than said first voltage, and a potential difference between said first voltage and said second voltage is greater than said source-drain breakdown voltage.

15. The method of claim 11, wherein each of said memory cells additionally comprises a select transistor connected in series with said storage transistor, said select transistor has a source and a drain and a source/drain-junction breakdown voltage equal to or greater than said first voltage, and a potential difference between said first voltage and said second voltage is larger than said source/drain-junction breakdown voltage.

16. The method of claim 11, wherein said method further comprises the steps of:

generating said first voltage from said supply voltage and said ground voltage; and

generating said second voltage from said supply voltage and said ground voltage.

17. The method of claim 11, wherein each of said memory cells additionally comprises a select transistor connected in series with said storage transistor, said select transistor has a source and a drain, and a source-drain breakdown voltage and a source/drain-junction breakdown voltage, and the source-drain breakdown voltage of the select transistor and the source/drain-junction breakdown voltage of the select transistor are each less than the potential difference between the first and second voltages.

18. The method of claim 11, and further including reading data from each of said memory cells by applying the supply voltage to the control gate and applying the ground to one of the source and drain during the reading of the data from the memory cell.

19. The method of claim 11, further comprising:

applying said ground voltage to at least one of the source and drain of the storage transistor or a non-selected memory cell,

whereby data is written in said selected memory cells simultaneously.

20. The method of claim 11, wherein said storage transitor also includes a substrate having a first conductivity type and provided therein with said source and drain, said source and drain being of a second conductivity type.